**New York Institute of Technology**

**School of Engineering and Computing Sciences**

NYIT Academy Summer Camp

VHDL Assignment 3: Counters

1. Consider the code below. It is a 2-bit synchronous counter with an asynchronous reset. The counter increments its count on each positive edge of the clock. If the reset is asserted low then the counter is reset to zero.

Library ieee;

Use ieee.std\_logic\_1164.all;

Use ieee.std\_logic\_arith.all;

Use ieee.std\_logic\_unsigned.all;

Entity Two\_Bit\_Up\_Counter is

Port (

Reset : in std\_logic;

Clock : in std\_logic;

Cnt\_out : out std\_logic\_vector(1 downto 0));

End Two\_Bit\_Up\_Counter;

Architecture Two\_Bit\_Up\_Counter\_Arch of Two\_Bit\_Up\_Counter is

Signal Cnt : std\_logic\_vector (1 downto 0);

Begin

Cnt\_out <= Cnt;

Count : Process ( Reset, Clock)

Begin

if Reset = '0' then

Cnt <= "00"; --asynchronous reset

elsif clock'event and Clock = '1' then

Cnt <= Cnt + "01";

end if;

End Process;

End Two\_Bit\_Up\_Counter\_Arch;

2. Implement the code by using ModelSim.

3. Design a 4-Bit Up Counter with an asynchronous reset.

4. Design a Sequence Counter. The counter has two control bits A and B and works as follows:

|  |  |  |
| --- | --- | --- |
| ***Control Bits*** | | ***Counter operation*** |
| ***A*** | ***B*** |
| *0* | *0* | *Even sequence counter:* 0000, 0010, 0100, 0110, 1000, 1010, 1100, 1110, then back to 0000 and repeat |
| *0* | *1* | *Odd sequence counter:* 0001, 0010, 0101, 0111, 1001, 1011, 1101, 1111, then back to 0001 and repeat |

All Laboratory Procedure must be done in Altera’s Quartus II software. Select Cyclone II EP2C35F672C6 as the target chip. All results must be display on Altera’s DE2 Development Board.